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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,826	07/19/2004	Pradip Mandal	IN 020001	8716

24737 7590 07/13/2005

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
TRAN, ANH Q	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/501,826	MANDAL, PRADIP	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2 rejected under 35 U.S.C. 102(e) as being anticipated by Yoshizaki et al (6,194,943).

Yoshizaki shows:

1. a voltage limiting semiconductor pass gate circuit (Fig. 2), comprising: a first transistor (1) being operatively operatively connected between an input node (Tin) and an output node (OUT) of the pass gate circuit, the first transistor having a control electrode being biased to a supply voltage (Vdd), characterized by the control electrode being biased to the supply voltage by two back-to-back connected diode elements (8, 9).

2. the diode elements are comprised of diode connected transistors.

4. An input I/O cell for use with integrated semiconductor circuit, the I/O cell having an input terminal (Tin), an output terminal (Tout) and at least one level detector circuit (7) coupled between the input terminal and the output terminal, characterized by a

semiconductor pass gate circuit in accordance with claim 1, coupled between the input terminal and the level detector circuit.

8. An integrated circuit compromising at least one input I/O cell in accordance with claim 4.

3. Claims 1, 2, 3 rejected under 35 U.S.C. 102(e) as being anticipated by Coddington (6,346,829)

Coddington shows:

1. a voltage limiting semiconductor pass gate circuit (Fig. 2), comprising: a first transistor (111) being operatively operatively connected between an input node (1) and an output node (8) of the pass gate circuit, the first transistor having a control electrode (2) being biased to a supply voltage (101), characterized by the control electrode being biased to the supply voltage by two back-to-back connected diode elements (104, 106).

2. the diode elements are comprised of diode connected transistors.

3. A semiconductor pass gate circuit according to claim 1, wherein the semiconductor pass gate circuit further comprises a second transistor (116) being operatively connected between the input node and the output node, the second transistor having a further control electrode (2) coupled to the control electrode of the transistor via the two back-to-back connected diode elements.

Claim Rejections - 35 USC § 103

4. Claims 1, 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (Fig. 1) in view of Yoshizaki et al (6,194943).

Applicant's Prior Art shows an I/O circuit (1) comprising: a pass transistor (9), a hysteresis inverter (4), and inverter (5) coupled between an input terminal (2) and output terminal (3). Therefore, the prior art, figure 1, discloses the claimed invention except for a gate of the pass transistor is being biased to the supply voltage by two back-to-back connected diode elements.

Yoshizaki discloses that it is known in the art to provide the gate of the pass transistor with two back-to-back connected diode elements (2 & 4, Fig. 1) biased the supply voltage to it gate. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the gate of the pass transistor of the Applicant prior art with the two back-to-back connected diode elements of Yoshizaki, in order to prevent the input circuit of a voltage exceeding the break-down voltage of the gate oxide film of a transistor even if the circuit receives a high-voltage signal, and suppressing the increase in propagation delay even with a reduced power supply voltage.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

7/8/05